Faculty of Engineering and Built Environment

Cape Peninsula University of Technology

Department of Electrical, Electronic and Computer Engineering (DEECE)

Bachelor of Engineering Technology: Electrical Engineering

CONTROL SYSTEMS 3 (CSS370S)

FINAL PROJECT PART 1: GA1 EVALUATION

PROJECT V05: 74LS192 / 74LS47 TWO-DISPLAY CRUISE SPEED CONTROL SYSTEM

System Design and Development, Simulation, Truth Tables and Practical Implementation Discussion

Student Name: Surname and Initials

Student Number: Number

Lecturer: Dr N. Dube

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Declaration

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Full Names and Surname: .....

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Summary/Abstract

This report presents Project V05 of the CSS370S GA1 cruise speed control simulation. The project requires a practical electronic circuit solution with no microcontroller and no PLC. The required system must display the current speed up to a maximum of 10, switch a green indicator ON for speeds 0 to 5, switch a yellow/amber indicator ON for speeds 6 to 9, and flash a red indicator when the selected cruise speed or maximum-speed condition is reached.

Project V05 uses two 74LS192 BCD up/down decade counters, two 74LS47 BCD-to-seven-segment drivers for common-anode displays, 74LS08 pulse/reset gates, a 74LS85 comparator, 4071/4073 logic gates, a 2N3904 transistor/relay driver, and an NE555 flashing red LED stage. The additional XOR correction forces the green LED OFF when the display reaches 10, and the reset gate supports automatic reset at invalid 11 and high 99 conditions.

The solution was analysed using the uploaded circuit diagram and the updated truth-table pack. The results confirm that the speed display, green/yellow range indication, comparator-triggered red warning, maximum-speed display and automatic reset/limit logic meet the expected project behaviour.

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Table of Acronyms

Table A: Acronyms used in the report

Acronym	Meaning
BCD	Binary Coded Decimal
LED	Light Emitting Diode
IC	Integrated Circuit
LSB	Least Significant Bit
MSB	Most Significant Bit
NE555	555 timer integrated circuit used for flashing output
GA1	Graduate Attribute 1: Problem Solving

1. Introduction

The CSS370S GA1 project is performed to demonstrate the design and analysis of a practical electronic cruise speed control simulation. The project requires students to use electronic components and to divide the solution into functional stages before combining them into a complete system.

The aim of Project V05 is to implement a two-display speed-control circuit that can count up and down, display values from 00 to 10, indicate 0 to 5 with a green LED, indicate 6 to 9 with a yellow/amber LED, and produce a flashing red warning when the selected cruise speed or maximum-speed condition is reached.

The problem addressed by this project is how to satisfy the complete control requirement without using software logic. The design must therefore use counters, display drivers, combinational logic, comparator circuitry, a timer stage and reset/limit logic to meet the same behaviour normally expected from a programmed controller.

The Project V05 simulation shows that the required behaviour can be achieved with electronic components only. The final system displays the current speed, separates the speed ranges, enables red flashing through the comparator/maximum-speed logic, and resets invalid count states after the maximum display range.

2. System description

Project V05 is based on two 74LS192 BCD up/down decade counters. The unit counter produces the unit digit and the ten counter produces the tens state used to show 10. The outputs are decoded by 74LS47 drivers connected to common-anode seven-segment displays.

Figure 1 presents the complete Project V05 circuit used for the report. The circuit shows the UP, DOWN and reset inputs, the two 74LS192 counters, the two 74LS47 display drivers, the green/yellow range logic, the 74LS85 comparator, the transistor/relay stage and the NE555 red flashing circuit.

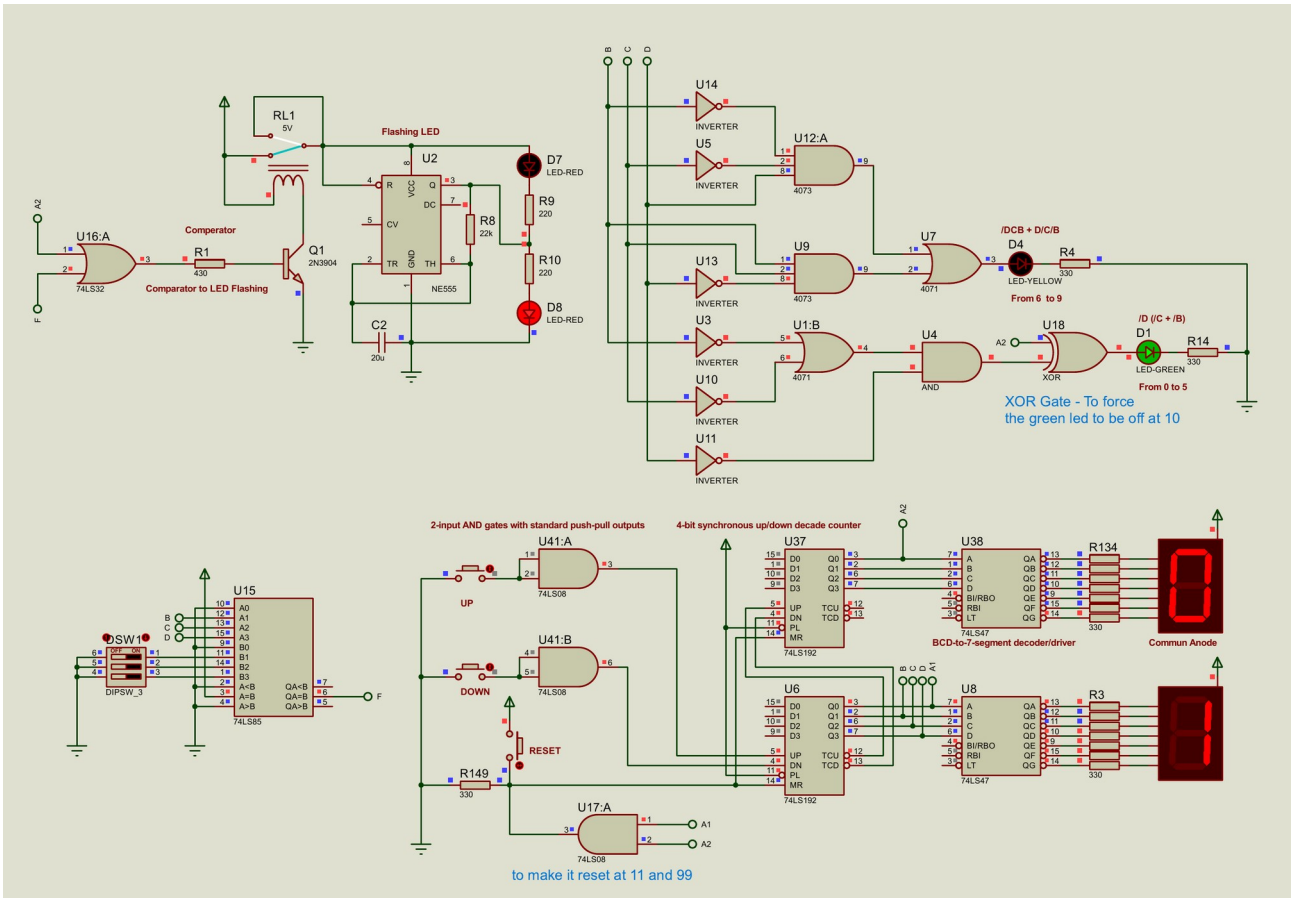

Figure 1: Project V05 74LS192 / 74LS47 cruise speed control circuit

Figure 2 presents the additional correction logic used in the updated Project V05 truth tables. The U17:A 74LS08 gate supports automatic reset at invalid 11 and high 99 states, while the U18 XOR gate forces the green LED OFF when the tens state A2 is active at speed 10.

Figure 2: Additional notes supplied for this update. Left: U17:A 74LS08 reset gate to force reset at 11 and 99. Right: U18 XOR gate to make the green LED OFF at 10.

Figure 2: Added reset and XOR correction logic used in Project V05

Table 1 defines the required operating conditions used to judge the Project V05 circuit. These conditions are introduced before the detailed component and truth-table analysis because they form the basis of the design verification.

Table 1: Required operating conditions for Project V05

Condition	Required output
Speed 00 to 05	Green LED ON, yellow LED OFF. Red LED depends on comparator condition.
Speed 06 to 09	Yellow/amber LED ON, green LED OFF. Red LED depends on comparator condition.
Speed reaches selected set speed	Comparator output F enables the red flashing warning.
Speed reaches 10	Maximum speed is displayed. Green and yellow LEDs are OFF and red warning is available/enabled.
Attempted speed 11 or high invalid state	Automatic reset/limit logic clears or blocks the invalid state.

Table 2 identifies the main components in Project V05 and explains the role of each part of the solution.

Table 2: Main component function table for Project V05

Component / label	Part	Function in this solution
U6 and U37	74LS192	Unit and ten BCD up/down decade counters.
U8 and U38	74LS47	BCD-to-seven-segment decoders/drivers for common-anode displays.

U41:A and U41:B	74LS08	UP and DOWN pulse conditioning gates.
U17:A	74LS08	Automatic reset gate for invalid 11 and 99 conditions.
U15	74LS85	Compares selected cruise speed with current speed.
DSW1	DIPSW_3	Manual set-speed input for the comparator.
U9, U12:A, U7	4073 and 4071 gates	Create the yellow/amber range output for 06 to 09.
U4 and U18	AND and XOR gates	Create the corrected green output and force it OFF at 10.
Q1, RL1 and U2	2N3904, relay, NE555	Enable and flash the red warning LED when required.

2.1 Stage 1: Development and overall approach to solution of automated system

The Project V05 solution was developed as separate electronic stages. The first stage is the speed display stage because the rest of the system depends on the displayed speed value.

The unit counter counts from 0 to 9 and the tens counter allows the display to show 10. The 74LS47 drivers convert the BCD counter outputs into common-anode display outputs, where the active segment logic is LOW.

2.2 Stage 2: Development and solution of the analog detection/sensors stage

This project version simulates speed digitally using UP and DOWN push-button pulses. Therefore, a physical analog detector is not used in this specific circuit. The simulated speed input still represents the detector output concept because it produces the current speed value used by the control system.

A physical version could replace the push-button input with a sensor and signal-conditioning circuit. The rest of the Project V05 logic would then use the converted digital speed value in the same way that the current counter stage is used.

2.3 Stage 3: Development and solution of determination of increasing/decreasing speed

Increasing and decreasing speed are implemented using the UP and DOWN inputs of the 74LS192 counters. UP pulses increase the displayed speed and DOWN pulses decrease the displayed speed. The 74LS08 input gates support reliable push-button control paths.

The added reset logic is important because the system must show 10 but must not continue into 11 or higher invalid states. The U17:A gate detects the invalid reset condition and returns the display to a valid state.

2.4 Stage 4: Development and solution of relevant alarms/indicators/displays of the system

The indication stage includes two seven-segment displays, a green LED, a yellow LED and a red flashing warning LED. The green/yellow logic uses the BCD outputs from the unit digit and the A2 tens signal. This prevents speed 10 from being incorrectly treated as a unit digit 0 in the green range.

The red LED warning is controlled by the 74LS85 comparator and the A2 maximum-speed signal. The NE555 circuit is enabled when the red-enable signal is HIGH, producing a flashing red warning instead of a steady red indication.

2.5 Stage 5: Overall approach to system design and solution development

The complete solution combines the counter/display stage, indicator logic, comparator stage, timer stage and reset/limit stage. This structure demonstrates the stage-wise development required in the project brief.

The overall approach is suitable for GA1 because the design problem is broken into smaller functional sections, each section is verified by truth tables, and the final system is evaluated against the required project outputs.

3. Observations and results

Table 3 lists the important 74LS192 pins and the signal names used in the Project V05 explanation. This makes the counter connections clear before the operation truth tables are presented.

Table 3: 74LS192 counter pin and signal table

74LS192 pin	Label	Use in this circuit
5	UP	Receives the count-up pulse.
4	DN	Receives the count-down pulse.
14	MR	Master reset input driven by reset path and automatic reset detector.
11	PL	Parallel load input kept inactive during normal counting.
15, 1, 10, 9	D0, D1, D2, D3	Preset data inputs not used for normal counting.
3	Q0 / A	Least significant BCD output. Unit output is A1 and tens output is A2.
2	Q1 / B	Second BCD output.
6	Q2 / C	Third BCD output.
7	Q3 / D	Most significant BCD output.
12	TCU	Terminal count up output used for cascading counters.
13	TCD	Terminal count down output used for cascading counters.

Table 4 gives the counter control operation. The manual reset returns the display to 00, while the automatic reset/limit condition is used for invalid states beyond the maximum-speed requirement.

Table 4: Counter control truth table

UP button	DOWN button	RESET input	Counter action	Display result
0	0	0	Hold	Same speed remains displayed
1 pulse	0	0	Count up	Display increases by 1
0	1 pulse	0	Count down	Display decreases by 1
1	1	0	Invalid / avoid	Unstable or ambiguous control condition
X	X	1	Reset active	Display returns to 00

Table 5 defines the BCD pattern used by each 74LS192 decade counter.

Table 5: 74LS192 BCD counter truth table

Decimal	D	C	B	A	BCD D C B A	Display
0	0	0	0	0	0000	0
1	0	0	0	1	0001	1
2	0	0	1	0	0010	2
3	0	0	1	1	0011	3
4	0	1	0	0	0100	4
5	0	1	0	1	0101	5
6	0	1	1	0	0110	6
7	0	1	1	1	0111	7
8	1	0	0	0	1000	8
9	1	0	0	1	1001	9

Table 6 gives the 74LS47 common-anode display output table. For this display driver arrangement, logic 0 switches a segment ON and logic 1 switches a segment OFF.

Table 6: 74LS47 common-anode display truth table

Decimal	BCD D C B A	a	b	c	d	e	f	g	Display

0	0000	0	0	0	0	0	0	1	0
1	0001	1	0	0	1	1	1	1	1
2	0010	0	0	1	0	0	1	0	2
3	0011	0	0	0	0	1	1	0	3
4	0100	1	0	0	1	1	0	0	4
5	0101	0	1	0	0	1	0	0	5
6	0110	0	1	0	0	0	0	0	6
7	0111	0	0	0	1	1	1	1	7
8	1000	0	0	0	0	0	0	0	8
9	1001	0	0	0	0	1	0	0	9

Table 7 shows the required two-display range from 00 to 10. The result confirms that speed 10 is displayed as the maximum value and that green/yellow indicators are OFF at 10.

Table 7: Two-display 00 to 10 operating truth table

Speed	Ten BCD	Unit BCD	Ten display	Unit display	Green	Yellow	Meaning
00	0000	0000	0	0	1	0	Green range
01	0000	0001	0	1	1	0	Green range
02	0000	0010	0	2	1	0	Green range
03	0000	0011	0	3	1	0	Green range
04	0000	0100	0	4	1	0	Green range
05	0000	0101	0	5	1	0	Green range
06	0000	0110	0	6	0	1	Amber/yellow range
07	0000	0111	0	7	0	1	Amber/yellow range
08	0000	1000	0	8	0	1	Amber/yellow range
09	0000	1001	0	9	0	1	Amber/yellow range
10	0001	0000	1	0	0	0	Maximum speed displayed; green/yellow OFF

Table 8 verifies the green/yellow logic with the XOR correction. The A2 tens signal is LOW for 00 to 09 and HIGH at 10, so the XOR stage turns green OFF when the display reaches 10.

Table 8: Green/yellow logic with XOR correction

Speed	D	C	B	A	A2	Yellow	Raw Green	Corrected Green	Final output
00	0	0	0	0	0	0	1	1	Green ON
01	0	0	0	1	0	0	1	1	Green ON
02	0	0	1	0	0	0	1	1	Green ON
03	0	0	1	1	0	0	1	1	Green ON
04	0	1	0	0	0	0	1	1	Green ON
05	0	1	0	1	0	0	1	1	Green ON
06	0	1	1	0	0	1	0	0	Yellow ON
07	0	1	1	1	0	1	0	0	Yellow ON
08	1	0	0	0	0	1	0	0	Yellow ON
09	1	0	0	1	0	1	0	0	Yellow ON
10	0	0	0	0	1	0	1	0	Both OFF

Table 9 shows how the automatic reset and maximum-speed condition are handled. This is different from the normal manual reset because it responds to invalid count conditions.

Table 9: Automatic reset and maximum-speed truth table

Present display	UP pulse	Reset at 11	Reset at 99	Action
00 to 08	1	0	0	Count normally upward.
09	1	0	0	Advance to 10.

10	1	1	0	Attempted 11 is detected and reset/blocked.
11 attempted	X	1	0	Invalid state is cleared.
99 attempted/high state	X	X	1	High invalid state reset protection becomes active.
Any value	Manual reset = 1	X	X	Display returns to 00.

Table 10 gives the comparator decision used by the red flashing warning section. The 74LS85 comparator produces the comparison outputs needed to determine whether current speed is below, equal to or above the selected speed.

Table 10: 74LS85 comparator truth table

Current speed condition	QA>B	QA=B	QA<B	F	Red LED result before A2 override
Current speed < Set speed	0	0	1	0	OFF
Current speed = Set speed	0	1	0	1	Flashing
Current speed > Set speed	1	0	0	1	Flashing

Table 11 shows how the comparator output is combined with the A2 tens signal. This means the red LED can flash when the set speed is reached or when the maximum speed 10 is displayed.

Table 11: Comparator-to-red flashing enable truth table

F from comparator	A2 tens bit	RedEnable = F + A2	Meaning
0	0	0	Below set speed and not at maximum: red LED OFF
1	0	1	Selected cruise speed reached or passed: red LED FLASHING
0	1	1	Maximum speed 10 reached: red LED FLASHING
1	1	1	Comparator reached and maximum speed active: red LED FLASHING

Table 12 gives the final NE555 flashing-stage operation after the transistor and relay enable path. When RedEnable is HIGH, the NE555 astable circuit produces the flashing red output.

Table 12: NE555 flashing LED truth table

RedEnable input	Q1 transistor	Relay RL1	NE555 state	Red LED state
0	OFF	OFF / not energised	Disabled	OFF
1	ON	ON / energised	Enabled astable mode	FLASHING

Table 13 summarises the final operating behaviour of Project V05. It confirms that the circuit satisfies the required green, yellow, red flashing, maximum-speed and automatic reset functions.

Table 13: Final operating summary

Condition	Green LED	Yellow LED	Flashing red LED	Display result
Speed 0–5 and F = 0	ON	OFF	OFF	00 to 05 displayed
Speed 0–5 and F = 1	ON	OFF	FLASHING	Cruise set speed reached within low range
Speed 6–9 and F = 0	OFF	ON	OFF	06 to 09 displayed
Speed 6–9 and F = 1	OFF	ON	FLASHING	Cruise set speed reached within higher range
Speed 10	OFF	OFF	FLASHING	Maximum speed displayed
Attempted speed 11	OFF during reset	OFF during reset	Reset action	Automatic reset returns display to 00

4. Conclusion

Project V05 demonstrates a complete electronic cruise speed control simulation using 74LS192 counters, 74LS47 common-anode display drivers, 74LS08 reset and pulse gates, a 74LS85 comparator, logic gates, a transistor/relay driver and an NE555 flashing circuit. The solution avoids the use of a microcontroller or PLC.

The truth-table results confirm that the circuit displays speeds from 00 to 10, switches the green LED ON for speeds 0 to 5, switches the yellow LED ON for speeds 6 to 9, and forces both range LEDs OFF at speed 10. The XOR correction is essential because it prevents the unit digit 0 at speed 10 from incorrectly activating the green LED.

The red flashing LED is enabled when the comparator output is active or when the A2 maximum-speed signal is active. The automatic reset/limit logic supports the requirement that speed 10 must be displayed while preventing the circuit from remaining in invalid states such as 11 or high 99 conditions.

Bibliography

[1] Texas Instruments, “SN54192, SN54LS192, SN74192, SN74LS192 synchronous 4-bit up/down counters datasheet,” Texas Instruments.

[2] Texas Instruments, “SN74LS47 BCD-to-seven-segment decoders/drivers datasheet,” Texas Instruments.

[3] Texas Instruments, “SN74LS85 4-bit magnitude comparator datasheet,” Texas Instruments.

[4] Texas Instruments, “NE555 precision timer datasheet,” Texas Instruments.

[5] onsemi, “2N3904 NPN general-purpose amplifier datasheet,” onsemi.

Appendices

APPENDIX A: Truth-table pack used for Project V05

The detailed Project V05 truth-table packs are attached separately as new1_truth_tables.pdf and new1_truth_tables_updated_xor_reset.pdf. The main report includes the most relevant truth tables required to explain and verify the circuit operation.

APPENDIX B: Practical evaluation scheme

This appendix follows the GA1 practical evaluation focus: identifying the problem, contextualising the design, formulating strategies, implementing the practical solution, and evaluating the observed results.

APPENDIX C: Report evaluation scheme

This appendix follows the report evaluation focus: stage-wise solution development, implementation, observations, conclusion and professional presentation.