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CONTROL SYSTEMS 3 (CSS370S)

FINAL PROJECT PART 1: GA1 EVALUATION

PROJECT V06: CD4029 / CD4511 TWO-DISPLAY CRUISE SPEED CONTROL SYSTEM

System Design and Development, Simulation, Truth Tables and Practical Implementation Discussion

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Declaration

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Summary/Abstract

This report presents Project V06 of the CSS370S GA1 cruise speed control simulation. The project requires an electronic circuit solution only, without a microcontroller and without PLC control. The required system must display speeds up to 10, show green for 0 to 5, show amber/yellow for 6 to 9, flash red when the selected cruise speed is reached, and include a logic-based cruise reset rather than only a normal reset button.

Project V06 uses two CD4029 BCD up/down counters, two CD4511 BCD-to-seven-segment latch/decoder/drivers for common-cathode displays, a 74LS85 comparator, range logic gates, force carry/borrow logic at 09, an XOR correction for the green LED, a 2N3904 transistor/relay driver, and an NE555 flashing red LED circuit.

The report applies the supplied circuit and updated truth tables to explain the design stage by stage. The results confirm that the circuit can show the 00 to 10 operating range, switch the correct green and yellow indicators, force carry/borrow around the 09 boundary, disable green in the two-digit high state, and activate the red flashing warning when the comparator or maximum-speed condition is reached.

Table of Contents

Declaration

Summary/Abstract

Table of Figures (TOF)

Table of Tables (TOT)

Table of Acronyms

1. Introduction

2. System description

2.1 Stage 1: Development and overall approach to solution of automated system

2.2 Stage 2: Development and solution of the analog detection/sensors stage

2.3 Stage 3: Development and solution of determination of increasing/decreasing speed

2.4 Stage 4: Development and solution of relevant alarms/indicators/displays of the system

2.5 Stage 5: Overall approach to system design and solution development

3. Observations and results

4. Conclusion

Bibliography

Appendices

Table of Figures (TOF)

Figure 1: Project V06 CD4029 / CD4511 cruise speed control circuit

Figure 2: Added force carry/borrow and XOR green correction logic

Table of Tables (TOT)

Table 1: Required operating conditions for Project V06

Table 2: Main component function table for Project V06

Table 3: Important connection and signal table

Table 4: UP, DOWN and reset operation truth table

Table 5: CD4029 BCD output truth table

Table 6: CD4511 common-cathode display truth table

Table 7: Two-display 00 to 10 operating truth table

Table 8: Force carry/borrow at 09 truth table

Table 9: Green/yellow logic with XOR correction

Table 10: Automatic maximum-speed/high-state limit table

Table 11: 74LS85 comparator truth table

Table 12: NE555 flashing red LED truth table

Table 13: Final operating summary

Table of Acronyms

Table A: Acronyms used in the report

Acronym	Meaning
BCD	Binary Coded Decimal
LED	Light Emitting Diode
IC	Integrated Circuit
LSB	Least Significant Bit
MSB	Most Significant Bit
NE555	555 timer integrated circuit used for flashing output
GA1	Graduate Attribute 1: Problem Solving

1. Introduction

The CSS370S GA1 project is performed to demonstrate the design and evaluation of a practical cruise speed control simulation using electronic components. The project brief requires stage-wise development and does not allow a microcontroller or PLC solution.

The aim of Project V06 is to implement a two-display speed-control circuit that counts the simulated speed, displays 00 to 10, indicates 0 to 5 using a green LED, indicates 6 to 9 using a yellow/amber LED, and produces a flashing red warning when the selected cruise speed is reached.

The main design problem is to implement the display, indicator and reset behaviour using hardware logic. The system must be able to show 10 as the maximum speed without allowing the circuit to operate normally in invalid states such as 11 or high two-digit values.

Project V06 solves this problem using CD4029 counters, CD4511 common-cathode display drivers, gate logic for the speed ranges, forced carry/borrow logic at 09, a 74LS85 comparator and an NE555 flashing red LED stage.

2. System description

Project V06 uses two CD4029 counters to produce a two-digit speed display. The unit counter handles the unit digit and the tens counter allows the system to show the maximum speed of 10. The CD4511 display drivers convert the BCD outputs into active-HIGH seven-segment signals for common-cathode displays.

Figure 1 presents the complete Project V06 circuit used for this report. The schematic includes the CD4029 counters, CD4511 display drivers, the green/yellow range logic, the 74LS85 comparator, the NE555 flashing red stage and the extra logic used for carry/borrow and green correction.

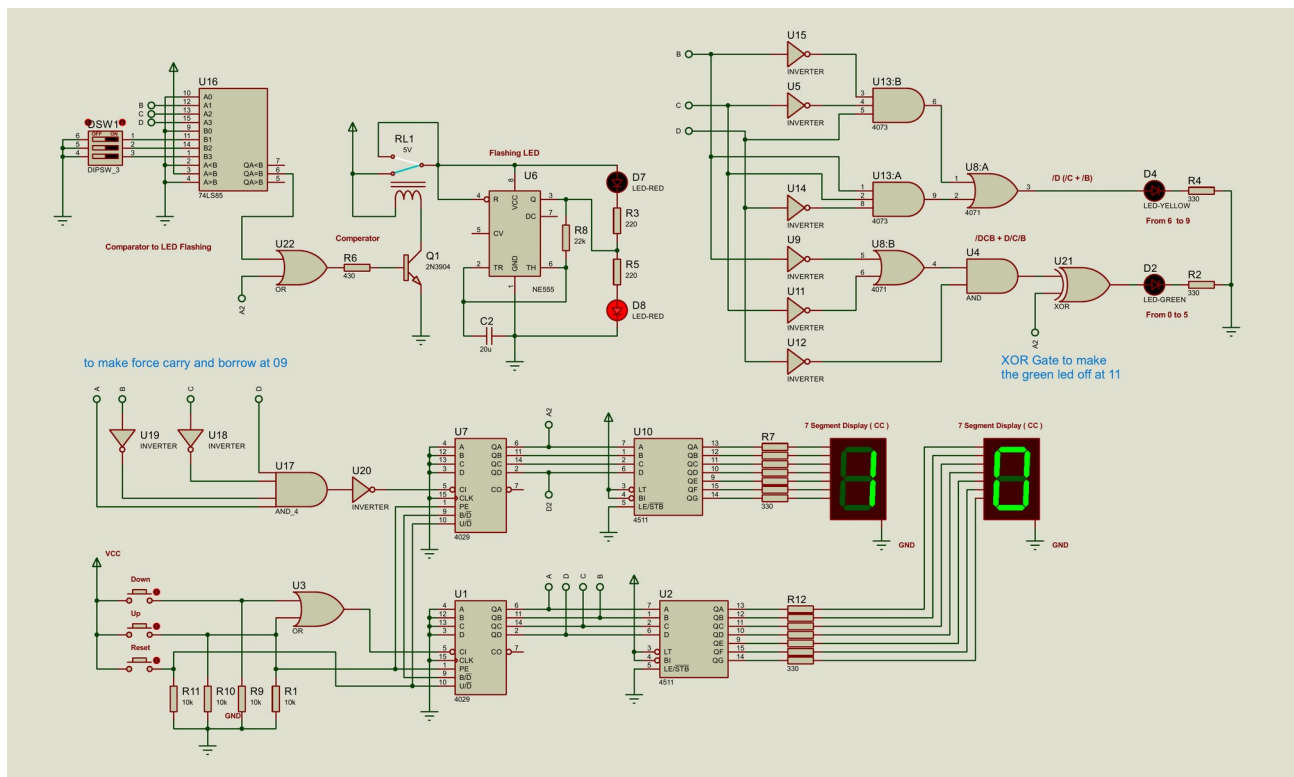


Figure 1: Project V06 CD4029 / CD4511 cruise speed control circuit

Figure 2 presents the additional logic details from the updated truth-table pack. The left section detects the unit digit 9 and forces carry/borrow at the 09 boundary, while the right section uses an XOR gate to make sure the green LED is OFF in the two-digit high state.

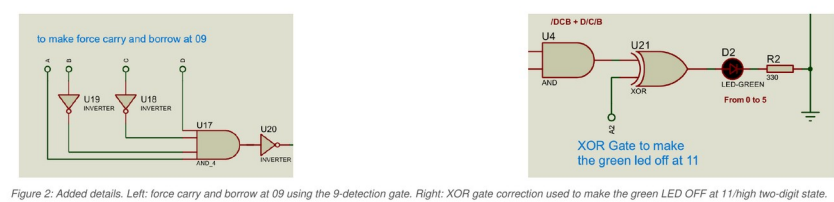


Figure 2: Added details. Left: force carry and borrow at 09 using the 9-detection gate. Right: XOR gate correction used to make the green LED OFF at 11/high two-digit state.

Figure 2: Added force carry/borrow and XOR green correction logic

Table 1 defines the operating conditions used to verify the circuit. These conditions are introduced first because the later truth tables are evaluated against these required outputs.

Table 1: Required operating conditions for Project V06

Condition	Required output
Speed 00 to 05	Green LED ON, yellow LED OFF. Red LED depends on comparator condition.
Speed 06 to 09	Yellow/amber LED ON, green LED OFF. Red LED depends on comparator condition.
09 boundary	Force carry/borrow logic becomes ready for the next transition.
Speed 10	Maximum speed displayed. Green and yellow LEDs are OFF.
Speed 11/high state	Green is forced OFF and reset/limit logic must clear or block the invalid state.

Table 2 summarises the main component groups used in the Project V06 solution.

Table 2: Main component function table for Project V06

Component / label	Part	Function in this solution
U1 and U7	CD4029	Unit and ten BCD up/down counters.
U2 and U10	CD4511	BCD-to-seven-segment latch/decoder/drivers for common-cathode displays.
U17, U18, U19, U20	AND_4 and inverters	Detect unit digit 9 and force carry/borrow at 09.
U21	XOR gate	Corrects the green LED output so it is OFF during the high/two-digit state.

U4, U8:A, U8:B, U13:A, U13:B	AND/OR/4073 logic	Generate green/yellow range logic.
U16	74LS85	Compares selected cruise speed with current speed.
DSW1	DIPSW_3	Manual cruise speed set input.
Q1, RL1 and U6	2N3904, relay, NE555	Enable and flash the red warning LED when set speed is reached.

2.1 Stage 1: Development and overall approach to solution of automated system

The overall Project V06 solution was developed as a two-digit electronic display and warning system. The display stage was developed first because the speed value is the main feedback signal for the rest of the logic.

The CD4029 counters provide BCD outputs for the current speed. The CD4511 drivers then convert the BCD values into visible digits on common-cathode seven-segment displays. The design can therefore show 00 to 10 instead of being limited to one digit.

2.2 Stage 2: Development and solution of the analog detection/sensors stage

Project V06 uses digital push-button input to simulate increasing or decreasing vehicle speed. A physical analog sensor is not included in this version of the circuit.

In a practical hardware extension, the push-button stage could be replaced by an analog detector and signal-conditioning stage followed by digital conversion. For this solution, the counter stage represents the available speed signal used by the rest of the control system.

2.3 Stage 3: Development and solution of determination of increasing/decreasing speed

The UP and DOWN controls determine whether the displayed speed increases or decreases. The U3 OR gate combines pulse paths into the counter clock section, while the CD4029 direction input determines the counting direction.

The added 09 detection logic improves the transition at the two-digit boundary. It detects the unit digit 9 using $A \cdot \text{NOT } B \cdot \text{NOT } C \cdot D$ and produces a carry/borrow control signal so that the counter can move correctly around 09 and 10.

2.4 Stage 4: Development and solution of relevant alarms/indicators/displays of the system

The indicator stage consists of the two seven-segment displays, the green LED, the yellow LED and the red flashing LEDs. The green/yellow logic is based on BCD range equations, while the XOR correction uses A2 to prevent the green LED from staying ON in the two-digit high state.

The red flashing stage is controlled by the 74LS85 comparator and NE555 timer. When the current speed equals or exceeds the selected set speed, the comparator output enables the transistor/relay path and the NE555 produces the flashing red warning.

2.5 Stage 5: Overall approach to system design and solution development

The complete Project V06 circuit combines the speed display, range indication, carry/borrow control, comparator warning and maximum-speed limiting functions. This gives a complete electronic solution without software control.

The design approach matches the GA1 problem-solving requirement because the problem is divided into stages, the stages are verified using truth tables, and the final behaviour is checked against the required output conditions.

3. Observations and results

Table 3 shows the most important signal connections for Project V06. It identifies how the counter, display driver, comparator and NE555 stages are linked.

Table 3: Important connection and signal table

Device	Pin / signal	Connection / use
CD4029 U1	QA, QB, QC, QD	Unit BCD outputs A, B, C, D to CD4511 U2 and LED/comparator logic.
CD4029 U7	QA / A2	Tens output used to show 10 and to disable green at maximum/high state.
CD4029	CLK	Clock pulses from the UP/DOWN input network.
CD4029	U/D	Direction control for increasing or decreasing speed.
CD4029	B/D	Set for BCD/decade counting mode.
CD4511 U2	A, B, C, D inputs	Receives unit BCD code from U1.
CD4511 U10	A, B, C, D inputs	Receives tens BCD code from U7.
CD4511	QA to QG	Segment outputs through 330 ohm resistors to common-cathode displays.
74LS85 U16	QA>B, QA=B	ORed to form comparator warning signal F.
NE555 U6	RESET / enable path	Activated through transistor/relay when warning enable is HIGH.

Table 4 gives the UP, DOWN and reset operation. The reset button is used for manual clearing, while the logic-based reset is used for the cruise maximum-speed condition.

Table 4: UP, DOWN and reset operation truth table

DOWN	UP	RESET	Clock from U3	Direction	Counter action	Display result
0	0	0	0	Previous	Hold	Same speed remains displayed
0	1 pulse	0	1 pulse	UP	Count up	Speed increases by 1
1 pulse	0	0	1 pulse	DOWN	Count down	Speed decreases by 1
1	1	0	1	Invalid	Not recommended	May behave incorrectly
X	X	1	X	X	Manual clear	Display returns to 00

Table 5 confirms the standard CD4029 BCD output pattern used for each digit.

Table 5: CD4029 BCD output truth table

Decimal	D	C	B	A	BCD D C B A	Display
0	0	0	0	0	0000	0
1	0	0	0	1	0001	1
2	0	0	1	0	0010	2
3	0	0	1	1	0011	3
4	0	1	0	0	0100	4
5	0	1	0	1	0101	5
6	0	1	1	0	0110	6
7	0	1	1	1	0111	7
8	1	0	0	0	1000	8
9	1	0	0	1	1001	9

Table 6 gives the CD4511 common-cathode display truth table. In this table, logic 1 means the segment is ON and logic 0 means the segment is OFF.

Table 6: CD4511 common-cathode display truth table

Decimal	BCD D C B A	a	b	c	d	e	f	g	Display
0	0000	1	1	1	1	1	1	0	0
1	0001	0	1	1	0	0	0	0	1
2	0010	1	1	0	1	1	0	1	2
3	0011	1	1	1	1	0	0	1	3
4	0100	0	1	1	0	0	1	1	4
5	0101	1	0	1	1	0	1	1	5
6	0110	1	0	1	1	1	1	1	6
7	0111	1	1	1	0	0	0	0	7
8	1000	1	1	1	1	1	1	1	8
9	1001	1	1	1	1	0	1	1	9

Table 7 shows the intended two-display range from 00 to 10. It confirms that the tens display remains 0 from 00 to 09 and becomes 1 at speed 10.

Table 7: Two-display 00 to 10 operating truth table

Speed	Ten BCD	Unit BCD	Ten display	Unit display	Green	Yellow	Meaning
00	0000	0000	0	0	1	0	Green range
01	0000	0001	0	1	1	0	Green range
02	0000	0010	0	2	1	0	Green range
03	0000	0011	0	3	1	0	Green range
04	0000	0100	0	4	1	0	Green range
05	0000	0101	0	5	1	0	Green range
06	0000	0110	0	6	0	1	Amber/yellow range
07	0000	0111	0	7	0	1	Amber/yellow range
08	0000	1000	0	8	0	1	Amber/yellow range
09	0000	1001	0	9	0	1	Amber/yellow range
10	0001	0000	1	0	0	0	Maximum speed displayed; green/yellow OFF

Table 8 verifies the force carry/borrow detection at unit digit 9. This signal becomes active only at the 09 boundary.

Table 8: Force carry/borrow at 09 truth table

Unit digit	D	C	B	A	N9 = A./B./C.D	U20 = NOT N9	Function
0	0	0	0	0	0	1	Normal count
1	0	0	0	1	0	1	Normal count
2	0	0	1	0	0	1	Normal count
3	0	0	1	1	0	1	Normal count
4	0	1	0	0	0	1	Normal count
5	0	1	0	1	0	1	Normal count
6	0	1	1	0	0	1	Normal count
7	0	1	1	1	0	1	Normal count
8	1	0	0	0	0	1	Normal count
9	1	0	0	1	1	0	Force carry/borrow boundary

Table 9 verifies the green/yellow LED logic with XOR correction. The additional 11 row shows that the green LED is forced OFF in the invalid high state.

Table 9: Green/yellow logic with XOR correction

Speed	D	C	B	A	A2	Yellow	Raw Green	Corrected Green	Final output
00	0	0	0	0	0	0	1	1	Green ON
01	0	0	0	1	0	0	1	1	Green ON
02	0	0	1	0	0	0	1	1	Green ON
03	0	0	1	1	0	0	1	1	Green ON
04	0	1	0	0	0	0	1	1	Green ON
05	0	1	0	1	0	0	1	1	Green ON
06	0	1	1	0	0	1	0	0	Yellow ON
07	0	1	1	1	0	1	0	0	Yellow ON
08	1	0	0	0	0	1	0	0	Yellow ON
09	1	0	0	1	0	1	0	0	Yellow ON
10	0	0	0	0	1	0	1	0	Both OFF at max
11	0	0	0	1	1	0	1	0	Invalid/ high state: Green OFF

Table 10 shows the maximum-speed and high-state limiting behaviour. This table explains how valid and invalid display states are handled.

Table 10: Automatic maximum-speed/high-state limit table

Display state	Valid?	Action
00 to 08	Valid	Normal counting.
09	Valid boundary	Force carry/borrow logic becomes ready.
10	Valid maximum	Maximum speed is displayed.
11	Invalid/high state	XOR correction keeps green OFF; reset/limit logic should clear or block this state.
99	Invalid/high state	High-state protection must reset or prevent continued counting.

Table 11 gives the comparator decision used to enable the red flashing LED. The output F becomes HIGH when the current speed is equal to or greater than the selected set speed.

Table 11: 74LS85 comparator truth table

Current speed condition	QA>B	QA=B	QA<B	F	Red LED
Current speed < Set speed	0	0	1	0	OFF
Current speed = Set speed	0	1	0	1	Flashing
Current speed > Set speed	1	0	0	1	Flashing

Table 12 shows the NE555 flashing stage. When the comparator output is HIGH, the transistor/relay path enables the NE555 astable mode and the red LED flashes.

Table 12: NE555 flashing red LED truth table

Comparator output F	Q1 / relay stage	NE555 state	Red LED state
0	OFF	Disabled or held reset	OFF
1	ON	Enabled astable mode	Flashing

Table 13 summarises the final operating behaviour of Project V06.

Table 13: Final operating summary

Condition	Green LED	Yellow LED	Red flashing LED	Display behaviour
Speed 00–05	ON	OFF	Depends on comparator set speed	Normal lower-speed range.
Speed 06–09	OFF	ON	Depends on comparator set speed	Amber/yellow range.
Speed 09 boundary	OFF	ON	Depends on comparator set speed	Force carry/borrow logic becomes active for the next transition.
Speed 10	OFF	OFF	Flashing if selected speed has been reached	Maximum speed displayed.
Speed 11 / high state	OFF by XOR correction	OFF	Depends after reset	Invalid/high state; reset/limit logic clears or blocks.

4. Conclusion

Project V06 demonstrates a complete electronic cruise speed control simulation using CD4029 counters, CD4511 common-cathode display drivers, range logic gates, a forced carry/borrow stage, a 74LS85 comparator, a transistor/relay driver and an NE555 flashing red LED circuit. The solution does not require a microcontroller or PLC.

The truth-table analysis confirms that the system displays speeds 00 to 10, turns the green LED ON for 00 to 05, turns the yellow LED ON for 06 to 09, and turns both range LEDs OFF at 10. The 09 detection logic supports the carry/borrow boundary, and the XOR correction prevents the green LED from remaining ON in the invalid two-digit high state.

The comparator and NE555 stage provide the required flashing red warning when the selected cruise speed is reached or exceeded. The maximum-speed and high-state tables show that the circuit can display 10 while treating 11 and 99 as invalid states that must be cleared or blocked by reset/limit logic.

Bibliography

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- [3] Texas Instruments, "SN74LS85 4-bit magnitude comparator datasheet," Texas Instruments.
- [4] Texas Instruments, "NE555 precision timer datasheet," Texas Instruments.
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Appendices

APPENDIX A: Truth-table pack used for Project V06

The detailed Project V06 truth-table packs are attached separately as new_project_truth_tables.pdf and new_project_truth_tables_updated_carry_xor.pdf. The main report includes the most important tables required for operation and verification.

APPENDIX B: Practical evaluation scheme

This appendix follows the GA1 practical evaluation focus: identifying the problem, contextualising the design, formulating strategies, implementing the practical solution, and evaluating the observed results.

APPENDIX C: Report evaluation scheme

This appendix follows the report evaluation focus: stage-wise solution development, implementation, observations, conclusion and professional presentation.