Faculty of Engineering and Built Environment

Cape Peninsula University of Technology

Department of Electrical, Electronic and Computer Engineering (DEECE)

Bachelor of Engineering Technology: Electrical Engineering

CONTROL SYSTEMS 3 (CSS370S)

FINAL PROJECT PART 1: GA1 EVALUATION

PROJECT V07: 74LS90 / 7447 TWO-DISPLAY CRUISE SPEED CONTROL SYSTEM WITH 4-BIT COMPARATOR

Updated Assumed Complete System Report with Truth Tables and Practical Implementation Discussion

Student Name: Surname and Initials

Student Number: Number

Lecturer: Dr N. Dube

Date: 19 June 2026

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Full Names and Surname: .....

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Summary/Abstract

This updated report presents Project V07 of the CSS370S GA1 cruise speed control simulation. The uploaded circuit is a basic two-display counter using two 74LS90 decade counters and two 7447 display drivers. The report assumes that the missing cruise-control sections have been added to complete the design.

The updated complete system keeps the existing 74LS90/7447 display stage and adds green/yellow range logic, a 74LS85 4-bit comparator, DIP-switch set-speed input, a comparator output combiner, an A2 maximum-speed override, a 2N3904 transistor/relay driver, an NE555 flashing red LED stage and automatic reset/limit logic.

The new 4-bit comparator section allows the current speed to be compared with a selected cruise set speed. For speeds 0 to 9, the unit BCD code can be used directly as the comparator A input. For speed 10, the design can either use an A2 maximum-speed override or add encoding logic to send 1010 to the comparator. The truth tables confirm the intended green, yellow, red flashing and maximum-speed behaviours.

Table of Contents

Table of Figures (TOF)

Table of Tables (TOT)

Table of Acronyms

Table A: Acronyms used in the report

Acronym	Meaning
BCD	Binary Coded Decimal
LED	Light Emitting Diode
IC	Integrated Circuit
LSB	Least Significant Bit
MSB	Most Significant Bit
NE555	555 timer integrated circuit used for flashing output
GA1	Graduate Attribute 1: Problem Solving

1. Introduction

The CSS370S GA1 project requires a practical electronic cruise speed control simulation. The design must be built using electronic components only, without a microcontroller and without a PLC. The required behaviour includes green indication for speeds 0 to 5, yellow/amber indication for speeds 6 to 9, flashing red indication when the selected cruise speed is reached, a visible maximum speed of 10 and a logic-based cruise reset.

Project V07 begins with a two-display counter circuit using 74LS90 decade counters and 7447 display drivers. The uploaded circuit provides the counting and display foundation, but it does not yet include the full comparator warning and cruise-control indicator system.

This updated report assumes the missing sections have been added. The most important update is the 74LS85 4-bit comparator section, which compares the current speed with a selected set speed from a DIP switch. The comparator output is then used to enable the NE555 flashing red warning.

The design problem is solved by using the existing 74LS90/7447 display stage as the speed display core, then adding the required range logic, comparator logic, flashing red warning and reset/limit logic around it.

2. System description

The uploaded Project V07 circuit contains two 74LS90 decade counters and two 7447 display drivers connected to common-anode seven-segment displays. The current circuit includes an UP input and RESET input. The assumed complete design adds the missing 4-bit comparator, set-speed input, green/yellow range logic, red flashing warning and cruise reset/limit sections.

Figure 1 presents the uploaded Project V07 circuit used as the starting point for the report. The figure shows the two-counter and two-display arrangement before the missing cruise-speed sections are added.

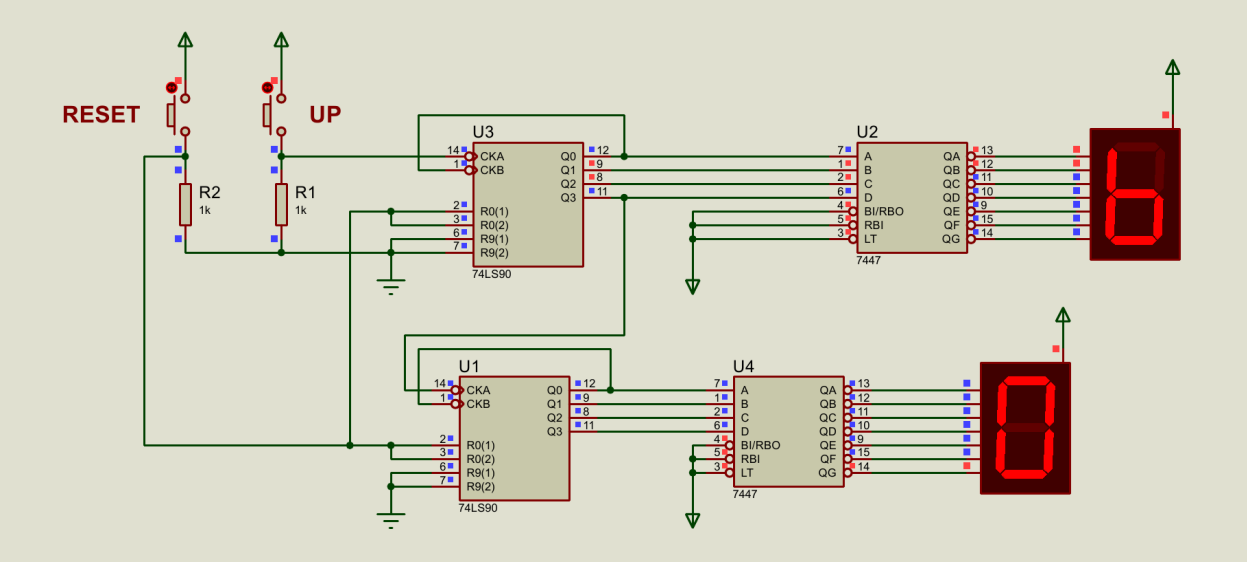

Figure 1: Project V07 uploaded 74LS90 / 7447 counter circuit

Figure 2 presents the assumed completed Project V07 structure. The added sections include the range-LED logic, 74LS85 4-bit comparator, DIP-switch set-speed input, NE555 flashing warning circuit and automatic maximum-speed reset/limit logic.

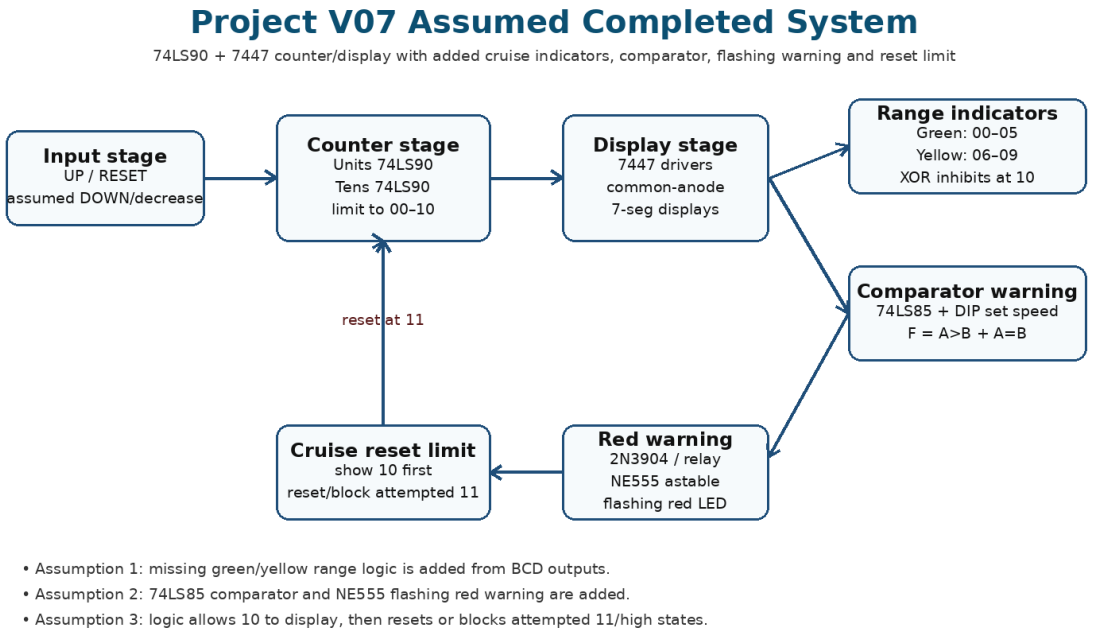

Figure 2: Assumed completed Project V07 with 4-bit comparator and warning sections

Table 1 states the assumptions used to complete Project V07 for reporting purposes. These assumptions are necessary because the uploaded schematic is still incomplete.

Table 1: Project V07 completion assumptions with 4-bit comparator

Assumed section	Function added to original circuit
Green range logic	Turns green ON for speeds 00 to 05.
Yellow range logic	Turns yellow ON for speeds 06 to 09.
4-bit comparator	Compares current speed with selected set speed using 74LS85.
A2 maximum override	Allows red warning at speed 10 if direct 1010 encoding is not added.
XOR/inhibit correction	Uses A2/tens signal so green is OFF at speed 10.
NE555 warning circuit	Flashes red LED when comparator warning is active.
Automatic 11 reset	Resets or blocks attempted 11 so the display does not remain above 10.

Table 2 identifies the main component groups used in the assumed completed Project V07 system.

Table 2: Main component function table for assumed complete Project V07

Component / label	Part	Function in completed Project V07
U1 and U3	74LS90	Unit and tens decade counters for two-display counting.
U2 and U4	7447 / 74LS47	BCD-to-seven-segment drivers for common-anode displays.
Added 74LS85	4-bit comparator	Compares current speed with selected cruise set speed.
Added DIP switch	4-bit set-speed input	Provides B3 B2 B1 B0 reference to comparator.
Added OR gate	Comparator output combiner	Combines QA>B and QA=B to form warning signal F.
Added A2 override	Tens/max signal	Enables red flashing at maximum speed 10 when required.
Added green/yellow gates	Logic gates	Generate 0–5 green and 6–9 yellow indicator ranges.
Added NE555 stage	Timer + driver	Flashes red LED when comparator warning is active.
Added reset/limit gate	AND/reset logic	Allows 10 to display and resets/blocks attempted 11.

2.1 Stage 1: Development and overall approach to solution of automated system

The system is developed around the existing counter/display section. The unit counter produces the unit digit and the tens counter produces the tens digit. The 7447 drivers convert the BCD outputs into segment outputs for common-anode displays.

The assumed complete design adds the missing cruise-control logic around this display core. The added logic uses the displayed count states to generate range indication, comparator warning and maximum-speed reset/limit control.

2.2 Stage 2: Development and solution of the analog detection/sensors stage

Project V07 uses push-button count input to simulate the speed signal. A physical analog speed detector is not included in the uploaded circuit. Therefore, the counter input is treated as the simulated speed input for the project.

In a final hardware version, a detector or sensor stage could generate speed pulses that feed the counter clock input. For this report, the UP pulse represents an increasing speed signal and the reset/limit logic represents the cruise-control boundary condition.

2.3 Stage 3: Development and solution of determination of increasing/decreasing speed

The uploaded circuit includes an UP input and RESET input. In the assumed complete Project V07 design, the UP input increases the displayed speed and the added reset/limit logic prevents the system from operating normally above the required maximum speed.

The maximum-speed limit is handled separately from the manual reset. The display must reach 10 first, then an attempted 11 condition is detected by the A2 and unit A1 logic and is reset or blocked.

2.4 Stage 4: Development and solution of relevant alarms/indicators/displays of the system

The indication stage includes the two seven-segment displays, green LED, yellow/amber LED and flashing red LED. The green LED indicates 00 to 05, the yellow LED indicates 06 to 09, and both range LEDs are OFF at 10.

The red warning is produced using the added 74LS85 4-bit comparator and NE555 flashing circuit. The 74LS85 receives the current speed on its A input and the selected set speed on its B input. The output F = QA>B + QA=B becomes active when the current speed is equal to or greater than the selected set speed.

2.5 Stage 5: Overall approach to system design and solution development

The final assumed complete Project V07 system combines the two-display counter, range indication, 4-bit comparator warning, flashing red output and automatic reset/limit logic. This creates a complete electronic solution from the incomplete starting circuit.

The approach satisfies the GA1 problem-solving requirement because the incomplete starting circuit is analysed, the missing functions are identified, the completion assumptions are stated, and the completed operation is verified with truth tables.

3. Observations and results

Table 3 shows how the 74LS85 4-bit comparator is connected in the assumed completed Project V07 circuit. This table is introduced before the comparator truth table because it explains the comparator input and output meanings.

Table 3: 4-bit comparator connection table

74LS85 pin group	Connection in completed Project V07
A3 A2 A1 A0	Current-speed 4-bit value. For 0–9 use unit BCD D C B A. For 10 use A2 maximum override or encoded 1010 logic.
B3 B2 B1 B0	Selected set-speed 4-bit reference from DIP switch.
I(A>B)	Tie LOW for single-comparator operation.
I(A=B)	Tie HIGH for single-comparator operation.
I(A<B)	Tie LOW for single-comparator operation.
QA>B	HIGH when current speed is greater than set speed.
QA=B	HIGH when current speed equals set speed.
QA<B	HIGH when current speed is lower than set speed.
RedEnable	RedEnable = QA>B + QA=B + A2(max). If direct 0–10 encoding is used, A2 max override may be omitted.

Table 4 gives the 74LS85 4-bit comparator truth table. The comparator output F is HIGH when the current speed is equal to or greater than the selected set speed.

Table 4: 74LS85 4-bit comparator truth table

I(A>B)	I(A=B)	I(A<B)	A vs B condition	QA>B	QA=B	QA<B	F = QA>B + QA=B	Red LED
0	1	0	A < B	0	0	1	0	OFF
0	1	0	A = B	0	1	0	1	Flashing
0	1	0	A > B	1	0	0	1	Flashing

Table 5 explains how the current speed is supplied to the comparator. For 0 to 9, the unit BCD code can be used directly. For 10, either an A2 maximum override or a direct 1010 encoder is required.

Table 5: Current-speed input code for the comparator

Displayed speed	Tens A2	Unit DCBA	74LS85 A input used	Max override	Meaning
00	0	0000	0000	0	Normal 4-bit compare
01	0	0001	0001	0	Normal 4-bit compare
02	0	0010	0010	0	Normal 4-bit compare
03	0	0011	0011	0	Normal 4-bit compare
04	0	0100	0100	0	Normal 4-bit compare
05	0	0101	0101	0	Normal 4-bit compare
06	0	0110	0110	0	Normal 4-bit compare
07	0	0111	0111	0	Normal 4-bit compare
08	0	1000	1000	0	Normal 4-bit compare
09	0	1001	1001	0	Normal 4-bit compare
10	1	0000 + A2	Unit 0000, A2 OR to RedEnable	1	Maximum-speed red enable

Table 6 shows the optional direct 4-bit encoding method. This is only required if the circuit is completed so that speed 10 is compared directly as 1010 instead of using the A2 override method.

Table 6: Optional direct 0 to 10 4-bit encoding table

Speed	Direct 4-bit value	A3	A2	A1	A0	Use
0	0000	0	0	0	0	Direct comparator code
1	0001	0	0	0	1	Direct comparator code
2	0010	0	0	1	0	Direct comparator code

3	0011	0	0	1	1	Direct comparator code
4	0100	0	1	0	0	Direct comparator code
5	0101	0	1	0	1	Direct comparator code
6	0110	0	1	1	0	Direct comparator code
7	0111	0	1	1	1	Direct comparator code
8	1000	1	0	0	0	Direct comparator code
9	1001	1	0	0	1	Direct comparator code
10	1010	1	0	1	0	Direct comparator code

Table 7 shows the DIP switch set-speed reference values for the 4-bit comparator.

Table 7: Set-speed DIP switch table

Set speed	DIP B3 B2 B1 B0	Meaning
6	0110	Red flashes when current speed >= 6
7	0111	Red flashes when current speed >= 7
8	1000	Red flashes when current speed >= 8
9	1001	Red flashes when current speed >= 9
10	1010	Red flashes when current speed >= 10

Table 8 summarises the current counter control behaviour from the uploaded 74LS90 circuit. The table also shows where automatic reset/limit logic is added.

Table 8: 74LS90 counter control truth table

UP pulse	Manual RESET	Automatic reset/limit	Counter action	Display result
0	0	0	Hold	Same value remains displayed.
1 pulse	0	0	Count up	Display increases by 1.
X	1	X	Manual reset	Display returns to 00.
X	0	1	Automatic cruise reset	Invalid value is cleared or blocked.

Table 9 shows the standard BCD sequence used by one 74LS90 decade counter.

Table 9: 74LS90 BCD counter truth table

Decimal	Q3/D	Q2/C	Q1/B	Q0/A	BCD DCBA	Display
0	0	0	0	0	0000	0
1	0	0	0	1	0001	1
2	0	0	1	0	0010	2
3	0	0	1	1	0011	3
4	0	1	0	0	0100	4
5	0	1	0	1	0101	5
6	0	1	1	0	0110	6
7	0	1	1	1	0111	7
8	1	0	0	0	1000	8
9	1	0	0	1	1001	9

Table 10 gives the 7447 common-anode display truth table. In this table, 0 means the segment is ON and 1 means the segment is OFF.

Table 10: 7447 common-anode display truth table

Digit	BCD DCBA	a	b	c	d	e	f	g	Display
0	0000	0	0	0	0	0	0	1	0
1	0001	1	0	0	1	1	1	1	1
2	0010	0	0	1	0	0	1	0	2
3	0011	0	0	0	0	1	1	0	3
4	0100	1	0	0	1	1	0	0	4
5	0101	0	1	0	0	1	0	0	5
6	0110	0	1	0	0	0	0	0	6
7	0111	0	0	0	1	1	1	1	7
8	1000	0	0	0	0	0	0	0	8
9	1001	0	0	0	0	1	0	0	9

Table 11 shows the intended 00 to 10 cruise-speed operating range after the missing completion logic is added.

Table 11: 00 to 10 cruise-speed operating truth table

Speed	Tens BCD	Units BCD	Tens display	Units display	Green	Yellow	Red warning	State
00	0000	0000	0	0	1	0	Depends on 4-bit comparator	0–5 green range
01	0000	0001	0	1	1	0	Depends on 4-bit comparator	0–5 green range
02	0000	0010	0	2	1	0	Depends on 4-bit comparator	0–5 green range
03	0000	0011	0	3	1	0	Depends on 4-bit comparator	0–5 green range
04	0000	0100	0	4	1	0	Depends on 4-bit comparator	0–5 green range
05	0000	0101	0	5	1	0	Depends on 4-bit comparator	0–5 green range
06	0000	0110	0	6	0	1	Depends on 4-bit comparator	6–9 yellow range
07	0000	0111	0	7	0	1	Depends on 4-bit comparator	6–9 yellow range
08	0000	1000	0	8	0	1	Depends on 4-bit comparator	6–9 yellow range
09	0000	1001	0	9	0	1	Depends on	6–9 yellow

							4-bit comparator	range
10	0001	0000	1	0	0	0	Flashing by A2/max or encoded compare	Maximum speed displayed

Table 12 verifies the assumed green/yellow indicator logic. The A2 tens signal is used to force green OFF at speed 10.

Table 12: Green/yellow indicator logic truth table

Speed	Unit DCBA	A2/Tens	Yellow	Green base	Final green	Indicator result
00	0000	0	0	1	1	Green ON
01	0001	0	0	1	1	Green ON
02	0010	0	0	1	1	Green ON
03	0011	0	0	1	1	Green ON
04	0100	0	0	1	1	Green ON
05	0101	0	0	1	1	Green ON
06	0110	0	1	0	0	Yellow ON
07	0111	0	1	0	0	Yellow ON
08	1000	0	1	0	0	Yellow ON
09	1001	0	1	0	0	Yellow ON
10	0000	1	0	1	0	Green/yellow OFF

Table 13 shows the logic-based cruise reset and maximum-speed limit operation. The system must display 10 first, then reset or block an attempted 11/high state.

Table 13: Automatic reset and maximum-speed limit truth table

Present display	UP pulse	Tens A2	Unit A1	Reset11 = A2.A1	Action
00 to 08	1	0	0/1	0	Counts normally upward.
09	1	0	1	0	Moves to 10 on next valid transition.
10	1	1	0	0	Maximum speed remains visible.
11 attempted	X	1	1	1	Automatic reset/limit clears or blocks invalid state.
Any value	Manual RESET = 1	X	X	X	Display returns to 00 for start-up/testing.

Table 14 gives the comparator matrix for speeds 00 to 10. A value of 1 means the red warning is active for the selected set speed.

Table 14: Comparator matrix for speeds 00 to 10

Current speed	Set 6	Set 7	Set 8	Set 9	Set 10	Red LED summary
0	0	0	0	0	0	OFF for set speeds 6–10
1	0	0	0	0	0	OFF for set speeds 6–10
2	0	0	0	0	0	OFF for set speeds 6–10
3	0	0	0	0	0	OFF for set speeds 6–10
4	0	0	0	0	0	OFF for set speeds 6–10
5	0	0	0	0	0	OFF for set speeds 6–10
6	1	0	0	0	0	Flashing for set speeds <= 6
7	1	1	0	0	0	Flashing for set speeds <= 7
8	1	1	1	0	0	Flashing for set speeds <= 8
9	1	1	1	1	0	Flashing for set speeds <= 9
10	1	1	1	1	1	Flashing for set speeds 6–10

Table 15 describes the assumed NE555 flashing red warning stage. When the warning enable is active, the NE555 operates in astable mode and flashes the red LED.

Table 15: NE555 flashing red warning truth table

RedEnable	Transistor/relay stage	NE555 state	Red LED state
0	OFF	Disabled or reset held	OFF
1	ON	Astable flashing mode	Flashing

Table 16 summarises the final Project V07 behaviour after the missing sections and 4-bit comparator are added.

Table 16: Final operating summary

Condition	4-bit comparator	Green LED	Yellow LED	Red LED	Display behaviour
Speed 00 to 05	A compared with B	ON	OFF	Depends on comparator	Low speed range.

Speed 06 to 09	A compared with B	OFF	ON	Depends on comparator	Higher speed range.
Current speed < set speed	QA<B=1	Range LED works	Range LED works	OFF	Cruise speed not reached.
Current speed = set speed	QA=B=1	Range LED works	Range LED works	Flashing	Cruise speed reached.
Current speed > set speed	QA>B=1	Range LED works	Range LED works	Flashing	Cruise speed passed.
Speed 10	A2 override or encoded 1010	OFF	OFF	Flashing if set/max active	Maximum speed displayed.
Attempted 11	Reset11=1	OFF after reset	OFF after reset	Reset/controlled	Automatic cruise reset clears invalid state.

4. Conclusion

Project V07 starts as a basic two-display 74LS90/7447 counter circuit. By assuming the missing cruise-speed-control sections and the 74LS85 4-bit comparator are added, the system becomes a complete electronic solution that satisfies the main project requirements.

The updated comparator section improves the design because it gives a clear hardware decision for when the red warning must flash. The current speed is connected to the comparator A input and the selected set speed is connected to the B input. When QA>B or QA=B is HIGH, the warning enable signal activates the red flashing circuit.

The truth-table results confirm that the green LED is active from 00 to 05, the yellow LED is active from 06 to 09, both range LEDs are OFF at 10, and the red LED flashes when the current speed reaches or exceeds the selected set speed. The maximum-speed reset logic allows the display to show 10 before clearing or blocking an attempted 11 state.

Bibliography

[1] Texas Instruments, “SN74LS90 decade, divide-by-twelve and binary counters datasheet,” Texas Instruments.

[2] Texas Instruments, “SN54LS47 / SN74LS47 BCD-to-seven-segment decoders/drivers datasheet,” Texas Instruments.

[3] Texas Instruments, “SN74LS85 4-bit magnitude comparator datasheet,” Texas Instruments.

[4] Texas Instruments, “NE555 precision timer datasheet,” Texas Instruments.

[5] onsemi, “2N3904 NPN general-purpose amplifier datasheet,” onsemi.

Appendices

APPENDIX A: Updated truth-table pack used for Project V07

The updated truth-table pack is attached separately as project_v07_truth_tables_with_4bit_comparator.pdf. It includes the 4-bit comparator connection table, comparator truth table, input coding options, set-speed table, comparator matrix, display tables, LED logic tables, reset table and NE555 flashing table.

APPENDIX B: Practical evaluation scheme

This appendix follows the GA1 practical evaluation focus: identifying the problem, contextualising the design, formulating strategies, implementing the practical solution and evaluating the observed results.

APPENDIX C: Report evaluation scheme

This appendix follows the report evaluation focus: stage-wise solution development, implementation, observations, conclusion and professional presentation.